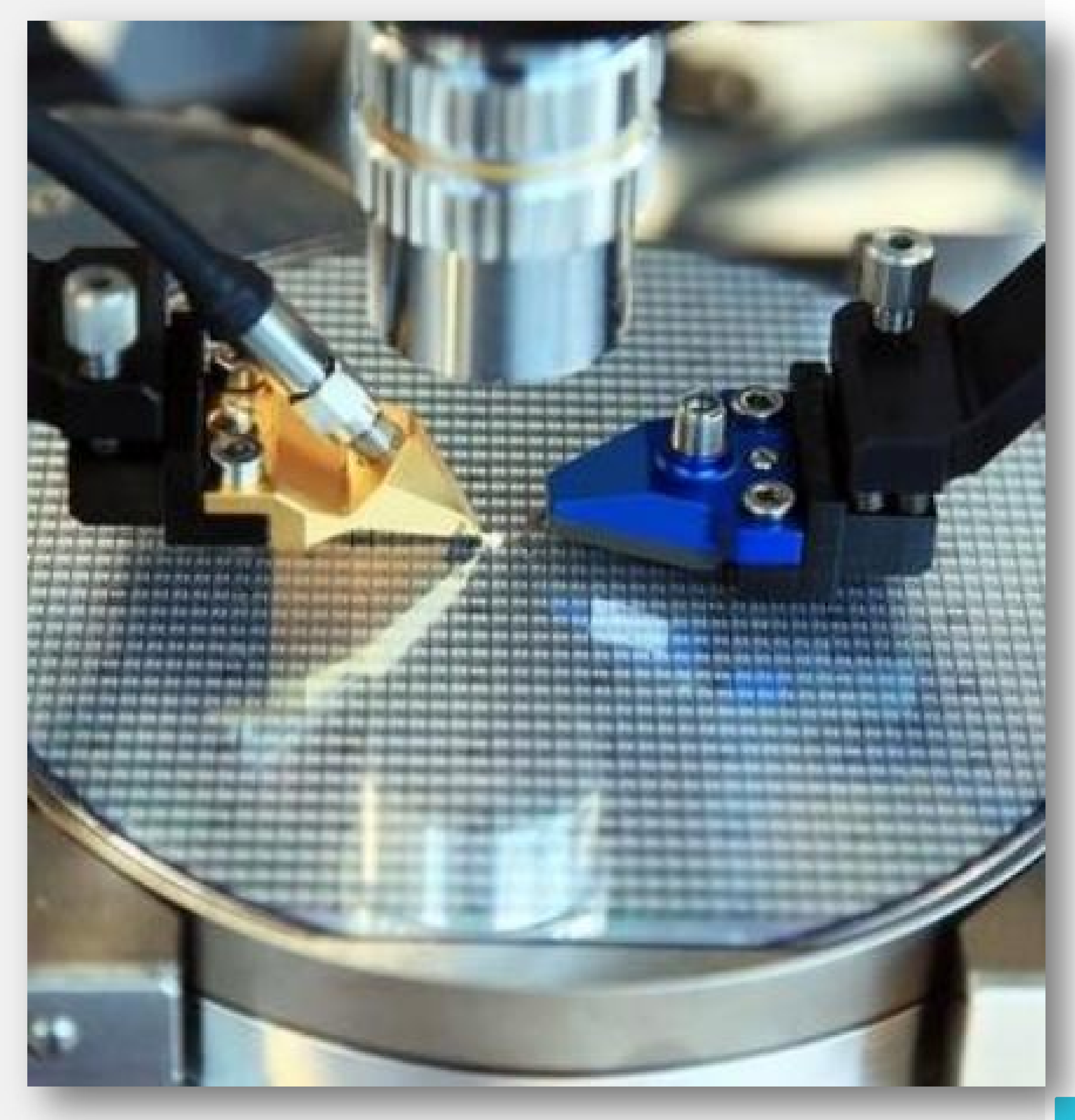
SSGsemi®
Company Profile
SSG Semiconductor 世晶半导体

About

SSGSEMI is a leading semi-conductor fabless design service company offers High Performance, High Quality Protection, Mixed Signal Analog Products to serve Automotive, Industrial, Consumer, Communications and Computing Segments.

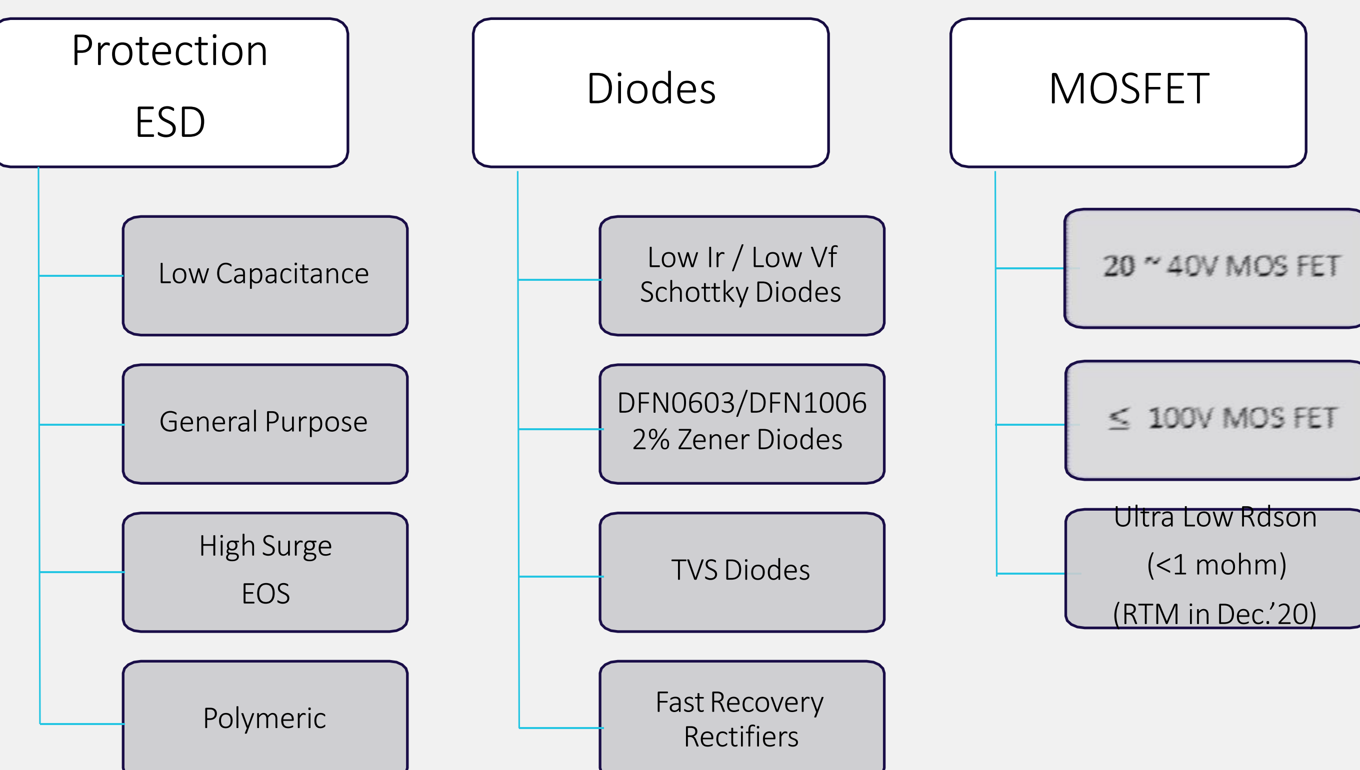
- 2014 Package, Assembly & Material research for low-pin counts device
- 2016 Built up the circuit design team in China
- 2016 Setup HQ office in Shenzhen, China

- **Head-quarter:** Shenzhen, CN
- **R&D Center**: CN and Taiwan
- Capital : RMB 10,000,000
- Employees : 28; R&D Engineers : 18
- Certification : ISO9001:2015, ISO14001, IATF 16949 (subcon MAF.)



SSGSEMI Focus Field

Product Portfolio



Key Achievements in Yr' 20– cont.

2. 1st USB4.0 ESD production device launched in industrial.

3. Launched the 3.3V ~ 60V high performance 400W TVS product lines in SOD-123 and SOD-323 package.

4. 7 high speed (ultra low cap.) ESD projects and 3 ultra low R_{DSON} , CSP MOS FET are under certified by US ODM customers.

5. 1+ billion shipments of TVS/ESD and Schottky (non-Automotive) in yr'19 and 50% YoY growth in Yr'20.

Plan in Yr 20

1. 200+ MOS FETs, 500+ ESD/EOS devices release to market
2. 50+ Schottky products launch in Yr'21
3. 50+ Zener products launch in Yr'21
4. Fulfill sales network in China

Technical Strength

Our key strengths

1. Strong semiconductor process knowledge and circuit design team (400+yrs design experience in diodes and analog design)
2. Industrial leading on low-cap, high speed and high surge diodes design
3. Industrial leading on ultra-low R_{DSON} design in MOS FET
4. Up streamline the supply chain (foundry, package and test), in order to improve the reliability and quality
5. Fully qualified by WW branding customers
6. Commit on R&D spending

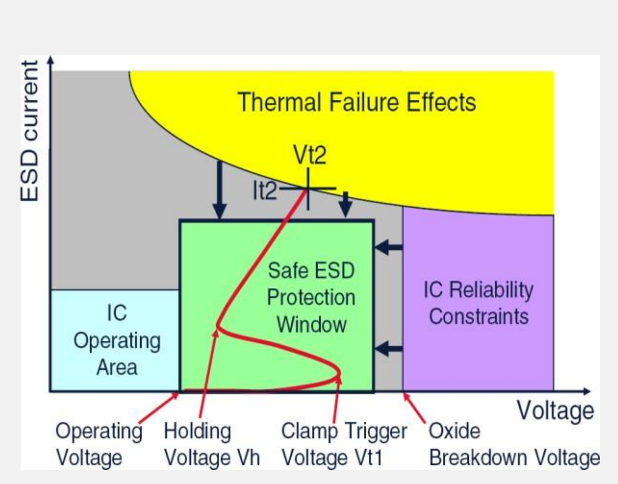
Today 's CMOS process drawbacks

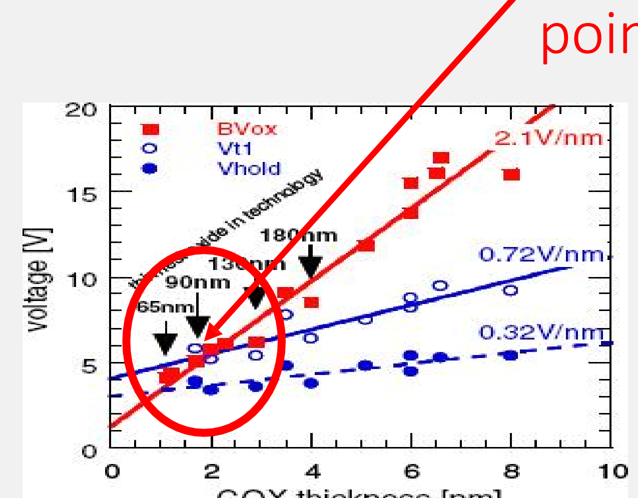
在互补式金氧半(CMOS)积体电路中，随着量产制程的演进，元件的尺寸已缩减到深次微米(deep-submicron)阶段，以增进积体电路(IC)的性能及运算速度，以及降低每颗晶片的制造成本。但随着元件尺寸的缩减，却出现一些可靠度的问题。

但是，CMOS 元件因为上述先进的制程技术以及缩得 更小的元件尺寸，使得次微米CMOS积体电路对静电放电 (Electrostatic Discharge ESD)的防护能力下降很多。但外界环境中所产生的静电并未减少，故CMOS积体电路因ESD而损伤的情形更为严重。

In order to keep the same level of protection, the system level protection has to relay on the external ESDs.

90nm technology is the sweet point for external ESD





How do we do to improve ESD

1. 制程上(Process Level)的改进方法
    a. ESD-Implant Process
    b. Modified ESD-Implant Process
    c. Silicided-Diffusion Blocking Process

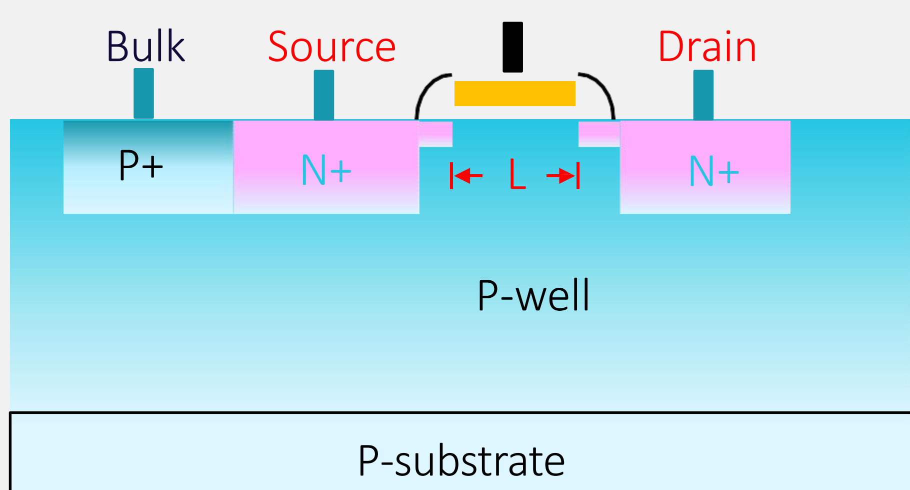
2. Architecture Design的改进方法
    a. Snapback
    b. SCR (Deep snapback)
    c. Modified SCR元件的设计
    d. Ultra-low cap. / low noise SCR元件的设计

3. 电路上(Circuit Level)的改进方法
    a. Gate-Couple
    b. N+P Gate-couple
    c. Modified N+P Gate with SCR design

制程上(Process Level)的改进方法

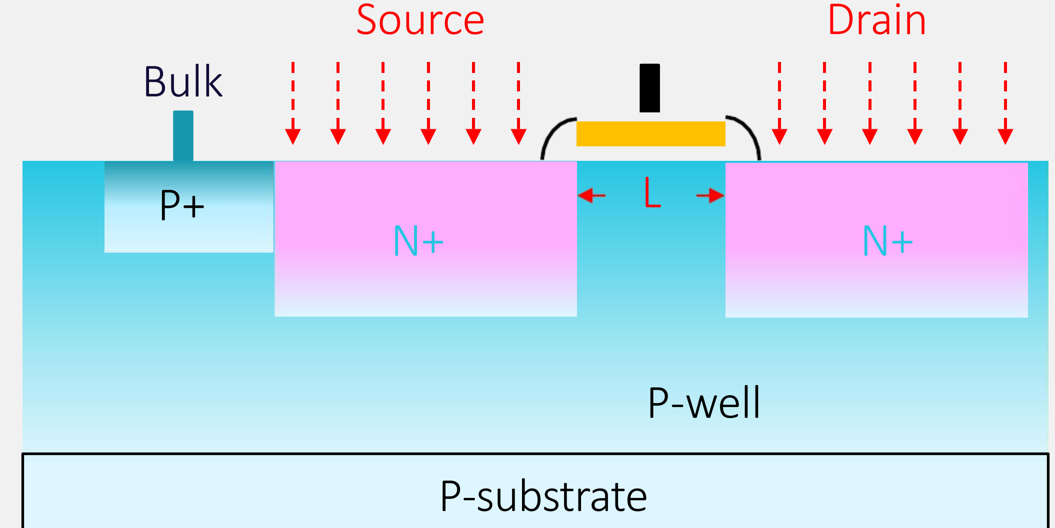
ESD Implant

Traditional Structure



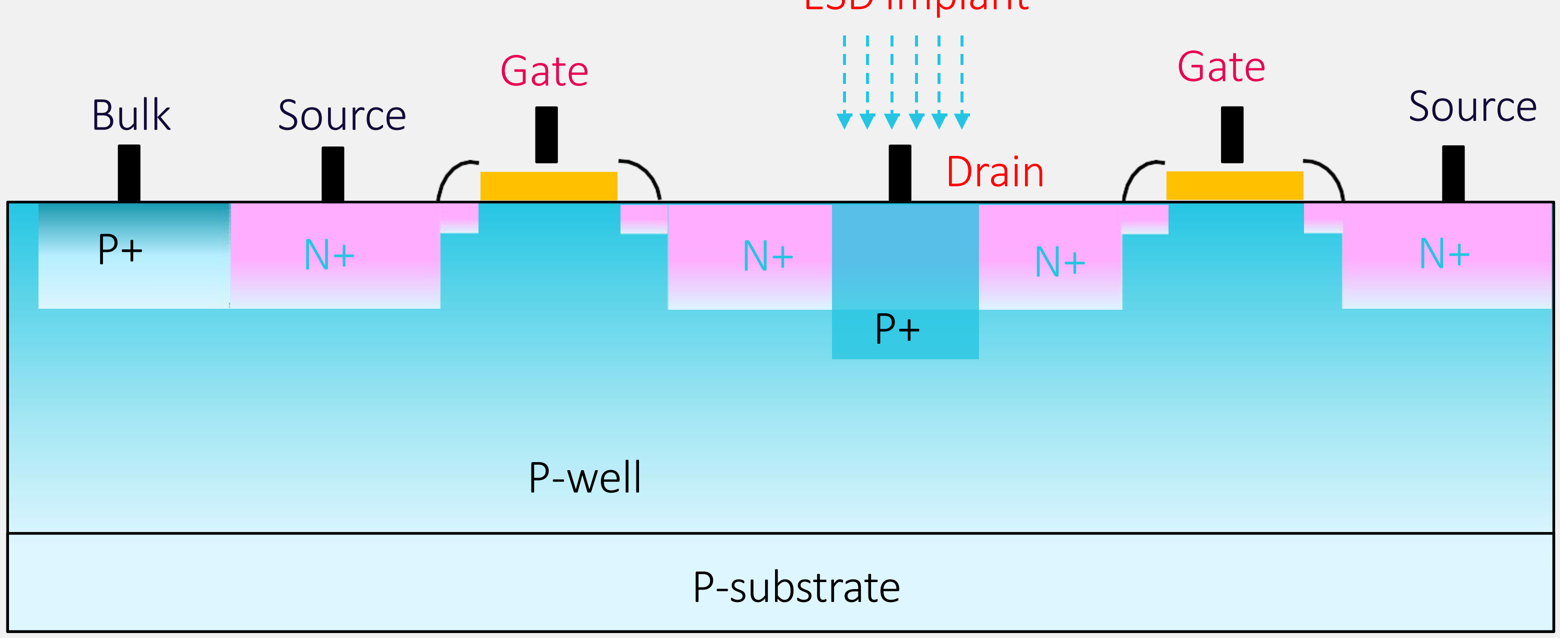
L=1.0um
Junction depth=0.18um
HBM ESD Robustness=1KV

ESD-Implant Structure



L=1.4um
Junction depth=0.22~0.25um
HBM ESD Robustness=4KV

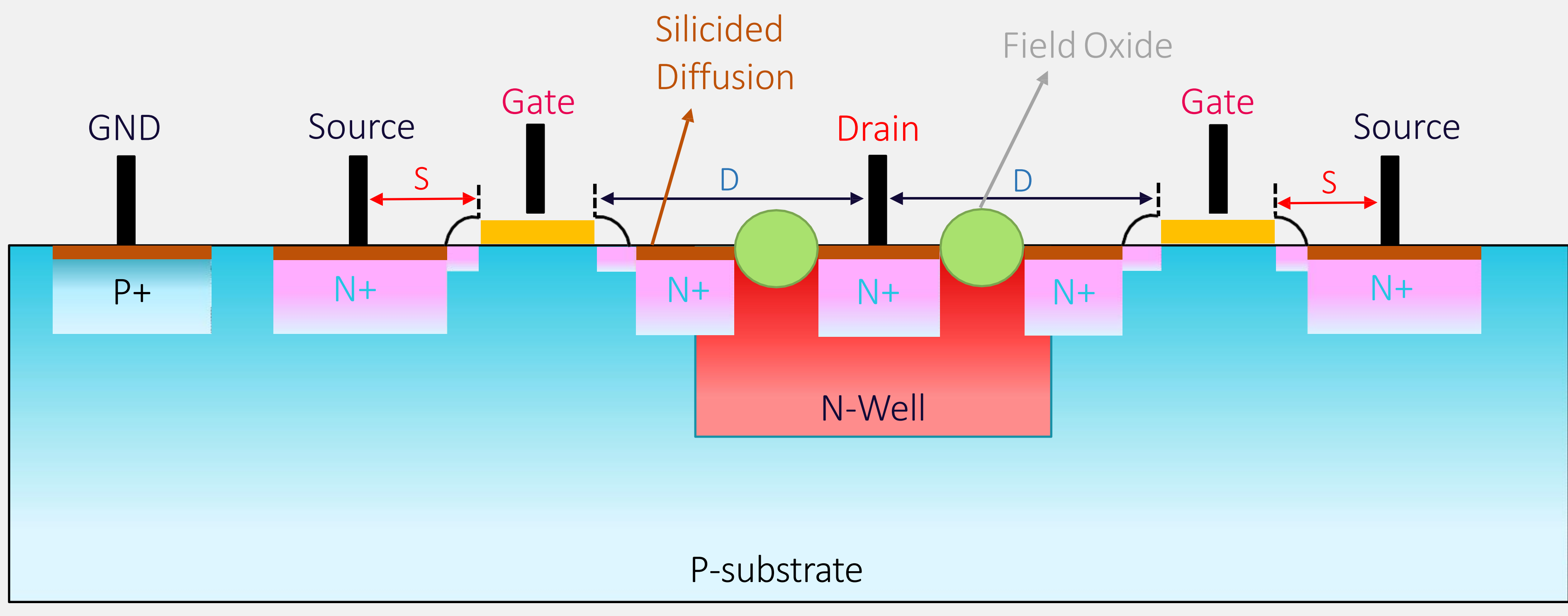
Modified ESD-Implant Structure



With silicide-blocking Mask

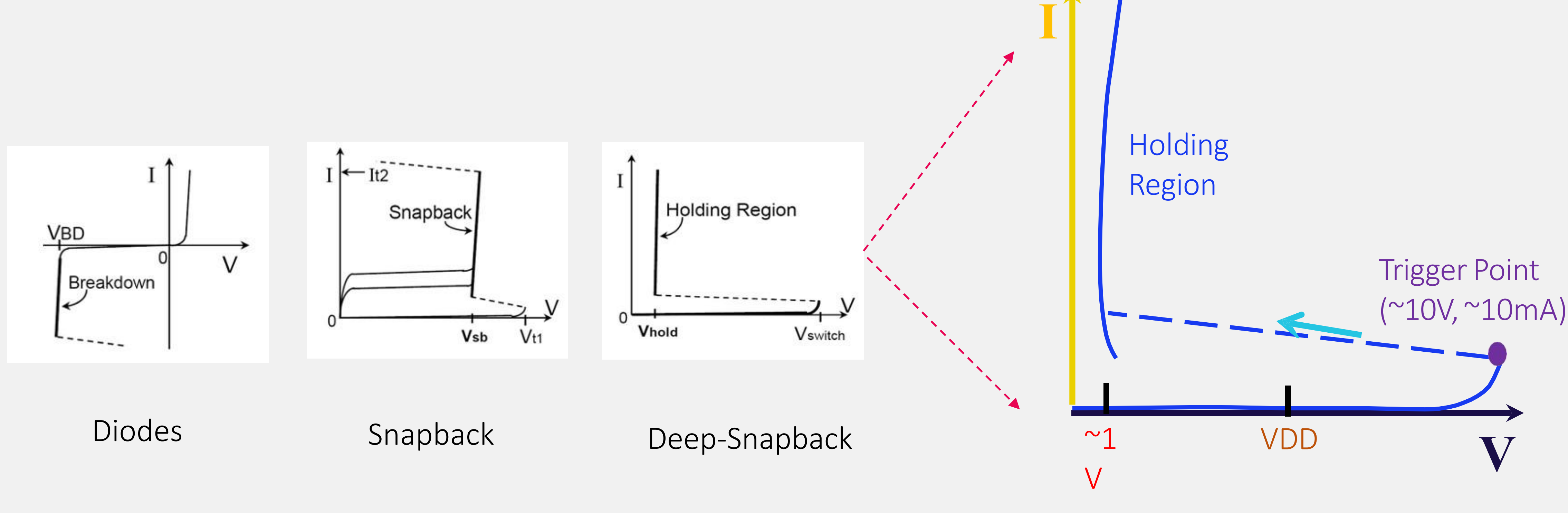
Conditions	W/O ESD	W/ESD	W/ESD
W(um)	490	420	600
L(um)	0.6	0.5	0.5
DGS(um)	2.5	3.4	1.8
VBD(V)	~8V	~6V	~6V
VESD(HBM)	2KV	5KV	4KV

Silicided-Diffusion Blocking Process

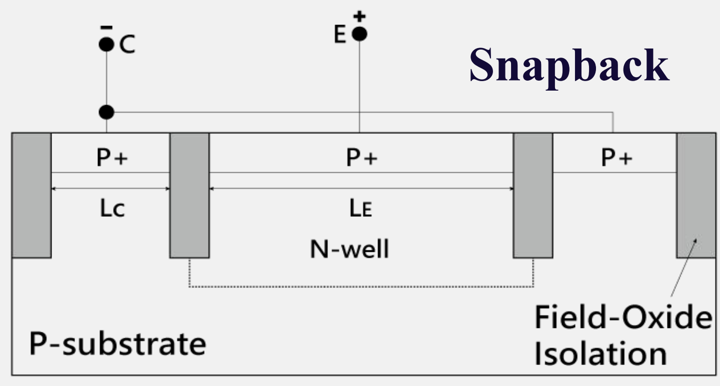


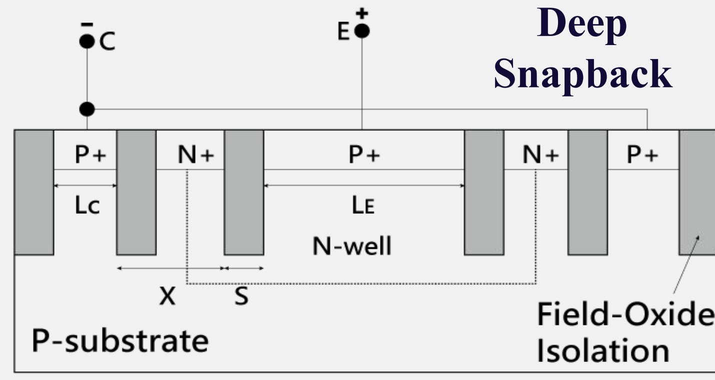
Architecture Design的改进方法

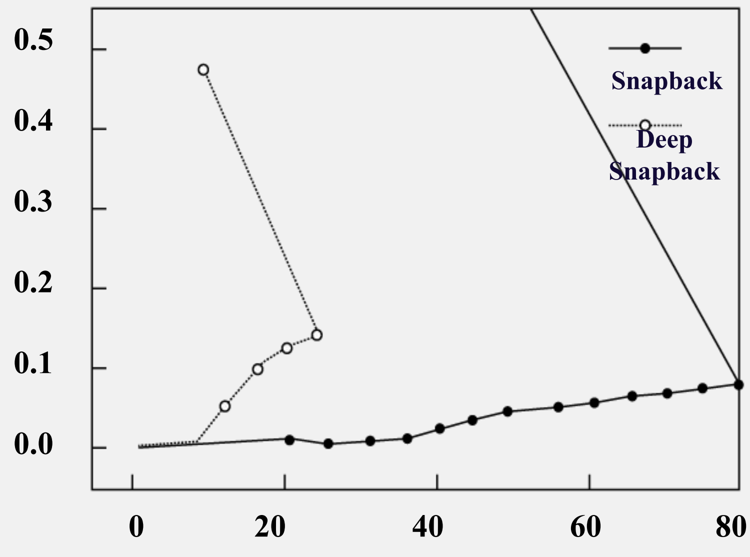
Popular ESD Architecture



Snapback vs Deep Snapback

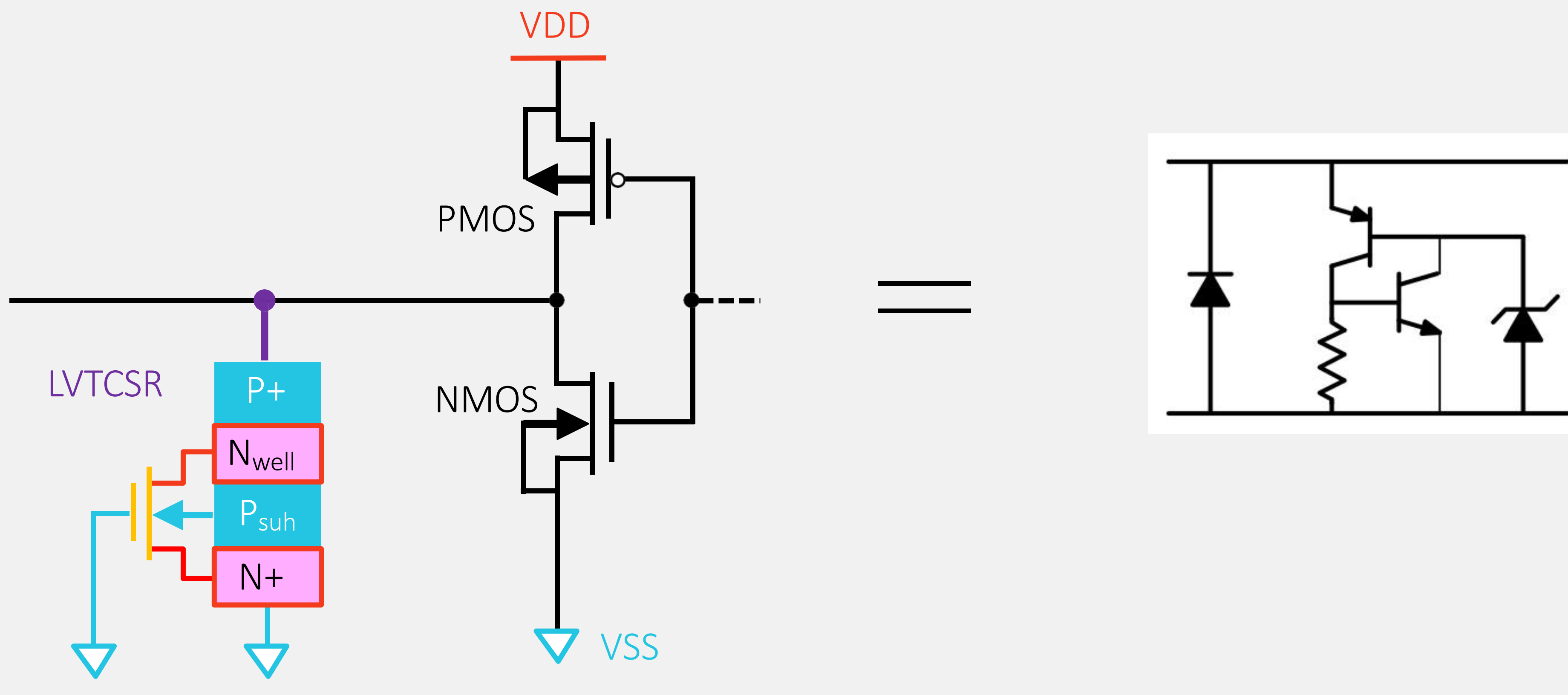




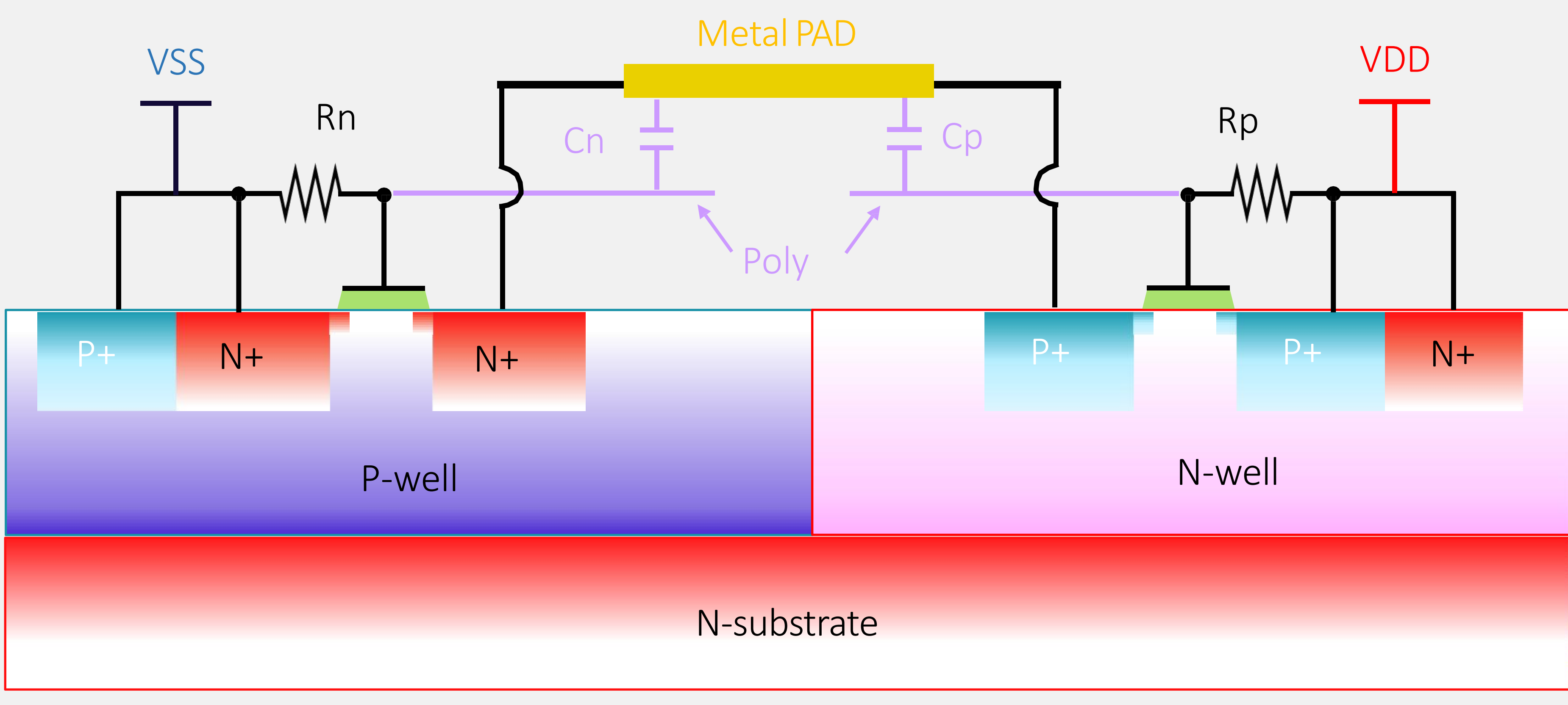


电路上(Circuit Level)的改进方法

Low-voltage-trigger Lateral SCR device for output ESD protection

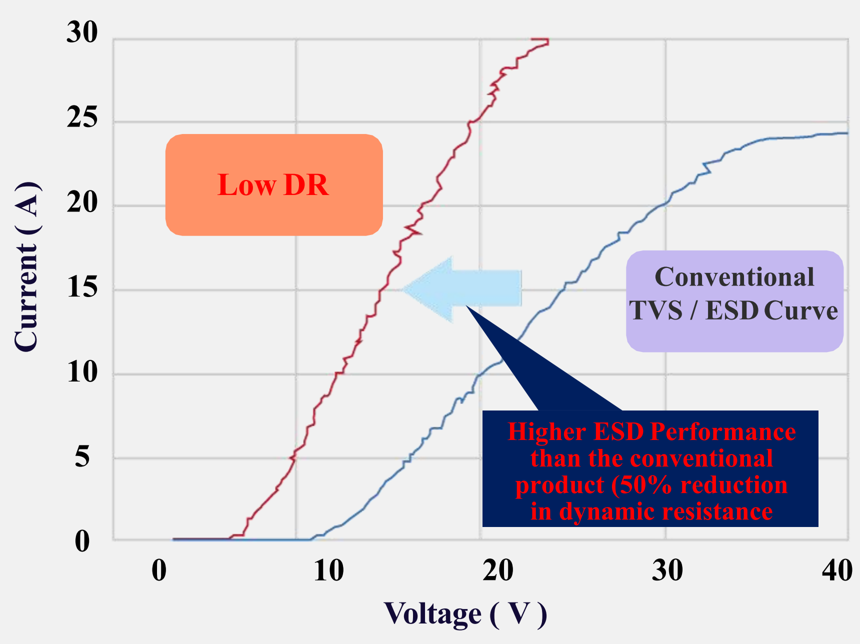


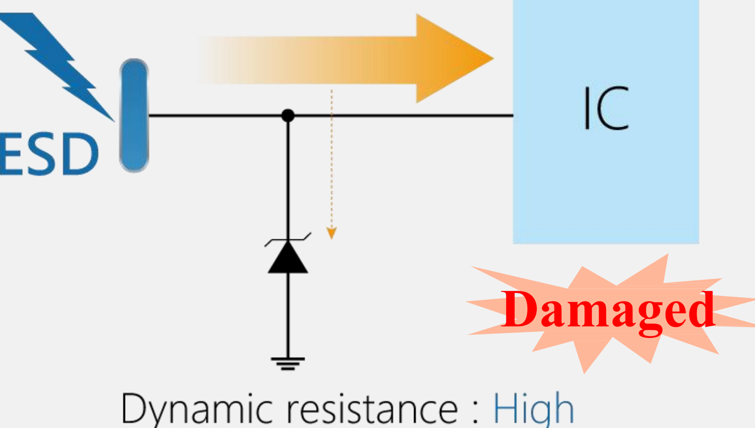
Schematic Cross-Sectional View of the Capacitor-Couple ESD Protection Circuit

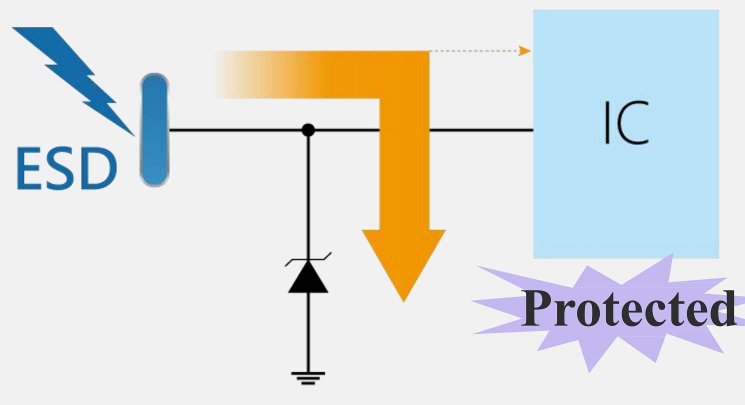


Other Important factors on ESD

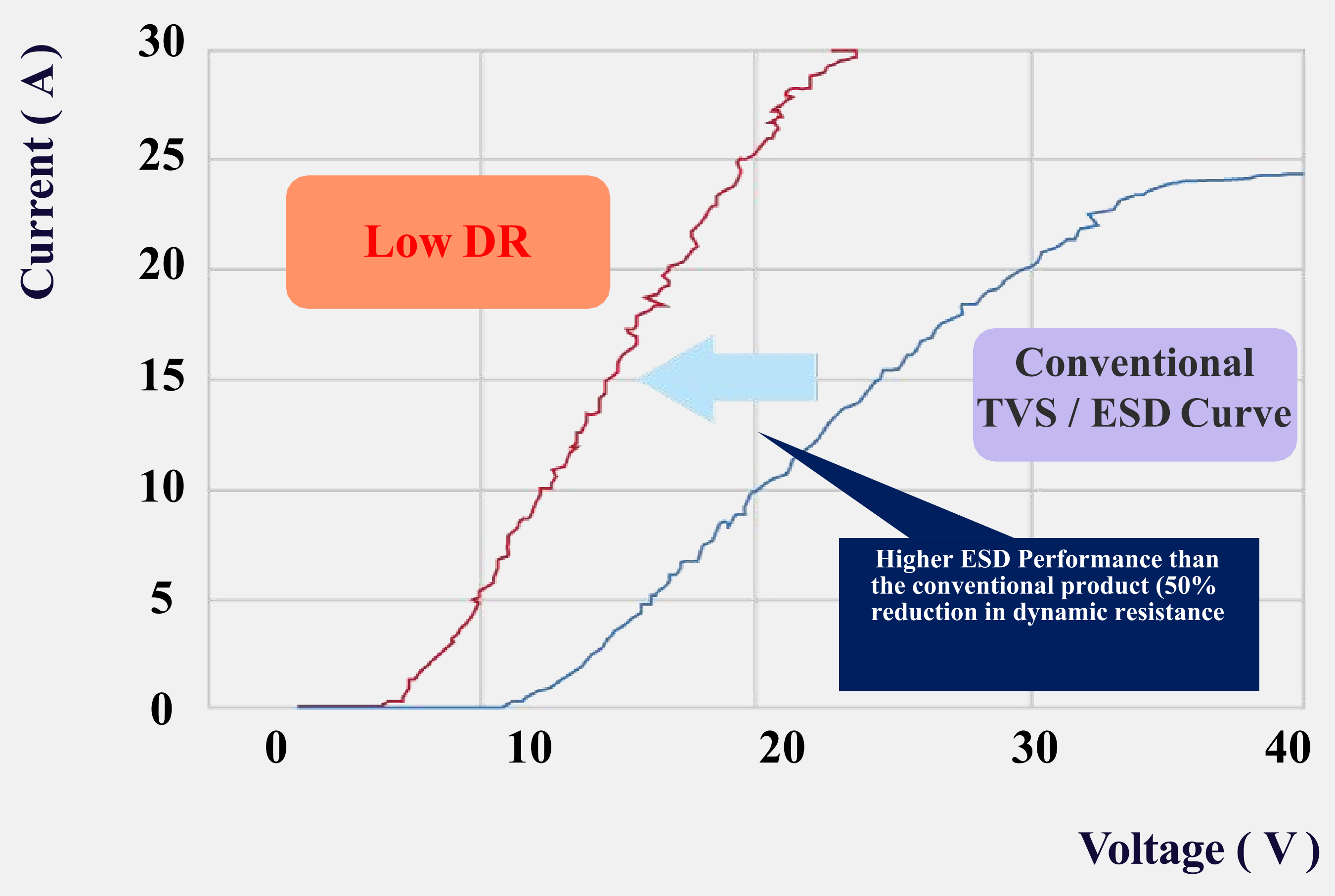
Dynamic Resistance







Dynamic Resistance



I_R – Leakage current

当系统没有受到静电等突波能量的攻击，正常运作在工作电压时，ESD的理想状态是OFF，不过实际上会有极小的漏电通过。

此时通过ESD元件的(漏电)电流(I_R)通常会小于1uA(10^{-6}A)。
元件的I_R越小越好，电路板上各式各样元件的I_R加总后就是系统不必要的电力浪费，通常会造成系统发烫，变成热能消散。

We choose the low resistor wafer and improved circuit to lower the IR, most of our devices are able to offer 10nA (typ.) mode.

V_C - Clamping Voltage

V_C (clamping voltage钳制电压)定义在通过ESD的电流I_R=1A。这数值已经是开闭状态时漏电流的一百万倍，是达到V_{BR}初开启状态时的1000倍。
此时可以视为元件防护全开，可将高达数千幅的静电电压压制在**V_C**这数值，使其无法再上升。
ESD元件的V_{CL}较低越好。V_{CL}较低表示系统遭受外来能量的瞬间所承受的最大电压比较低，于是冲击可以降低。
另一个角度看，V_{CL}较低的元件表示在相同电压之下通过的电流较大。这相当于排洪的水道比较宽，能量排除的速度较快。

Choosing the customized wafer and unique deep-implant process to lower the V_C.

Hero Devices

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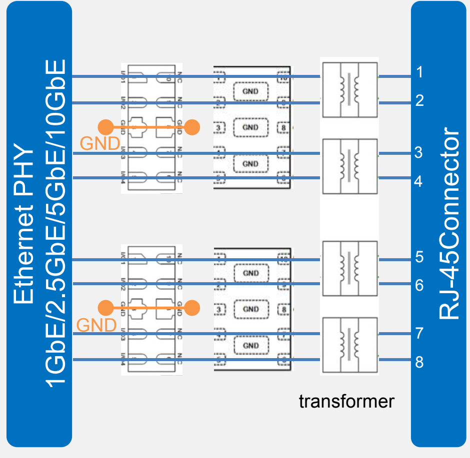
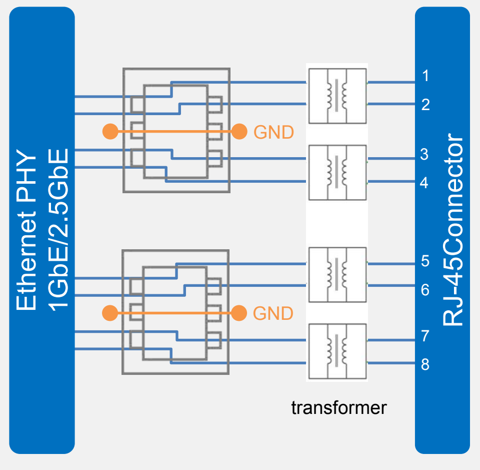
Ethernet Protection

Ethernet Solution 1:
Line to GND/Line to Line



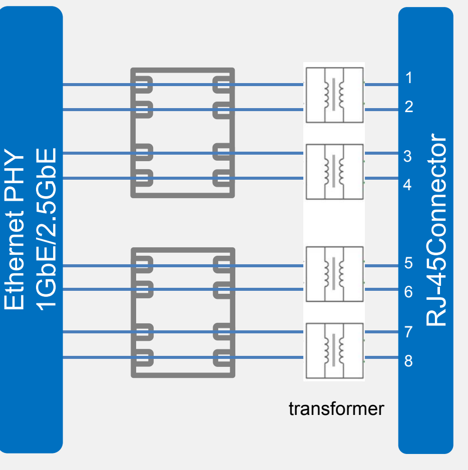
DFN2510-10L DFN3020-10L

Ethernet Solution 2:
Line to GND



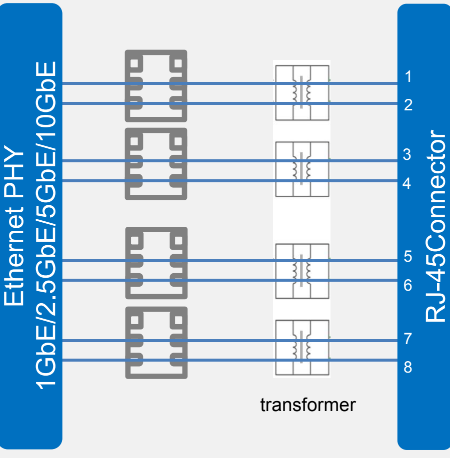
SOT-23-6L

Ethernet Solution 3:
Line to Line



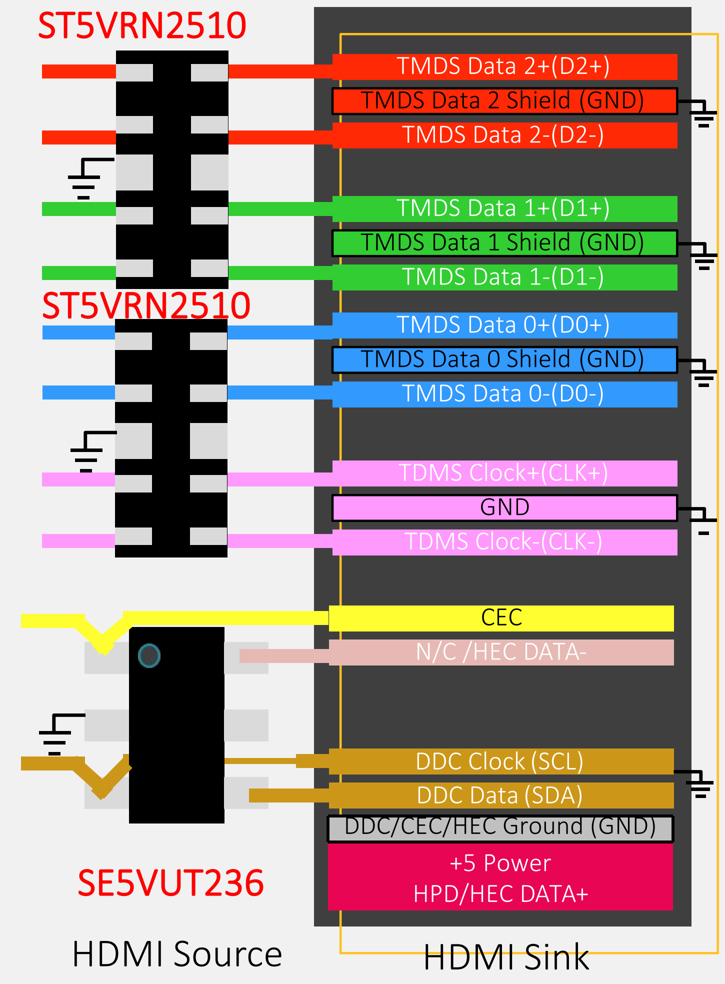
DFN2010-8L

Ethernet Solution 4:
Line to Line

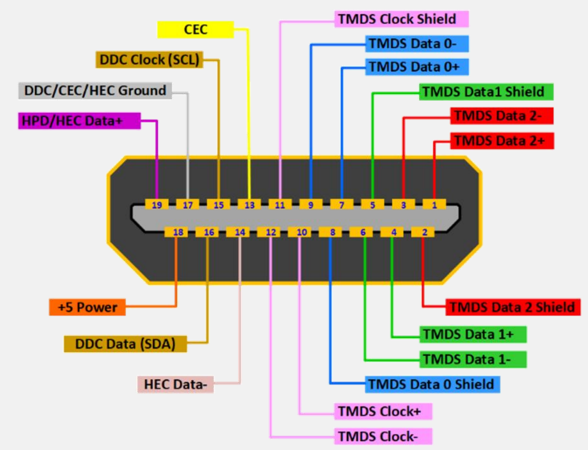


DFN1610-6L

HDMI 1.4 Application



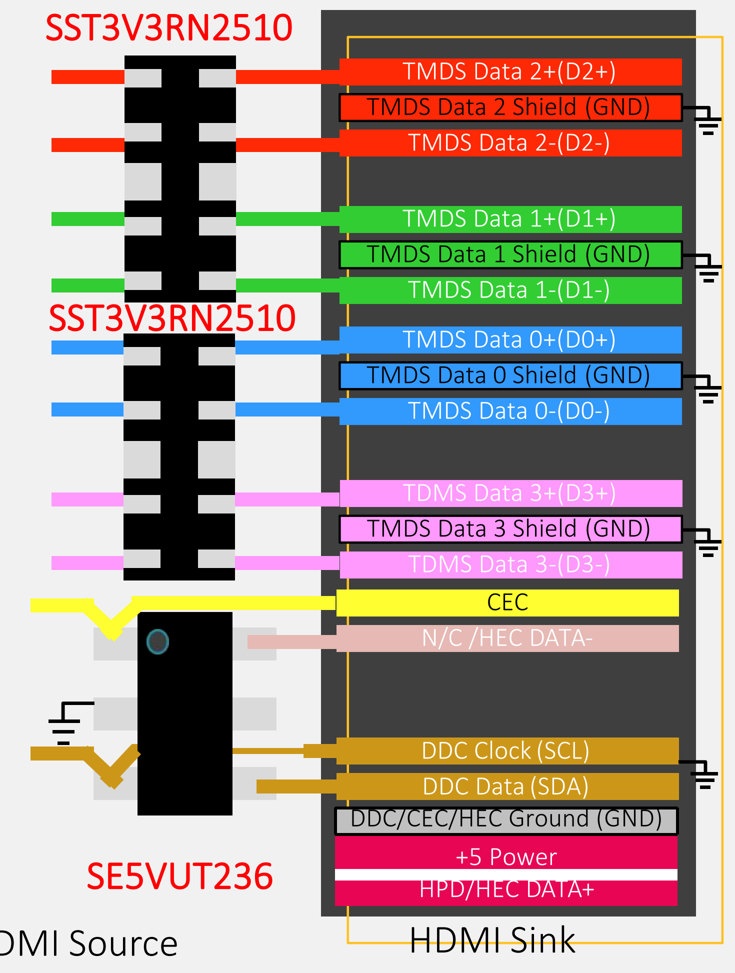
The flow-through package design



Recommend Part

P/N	Package	lines	Place
ST5VRN2510	DFN2510-10L	4	TMDS+ , TMDS- ,CLK
ST5VRN2510	DFN2510-10L	4	TMDS+ , TMDS- ,CLK
ST5VRN2510	SOT23-6L	4	CEC,SCL,SDA,HEC
SE5VUT236	SOT23-6L	4	CEC,SCL,SDA,HEC

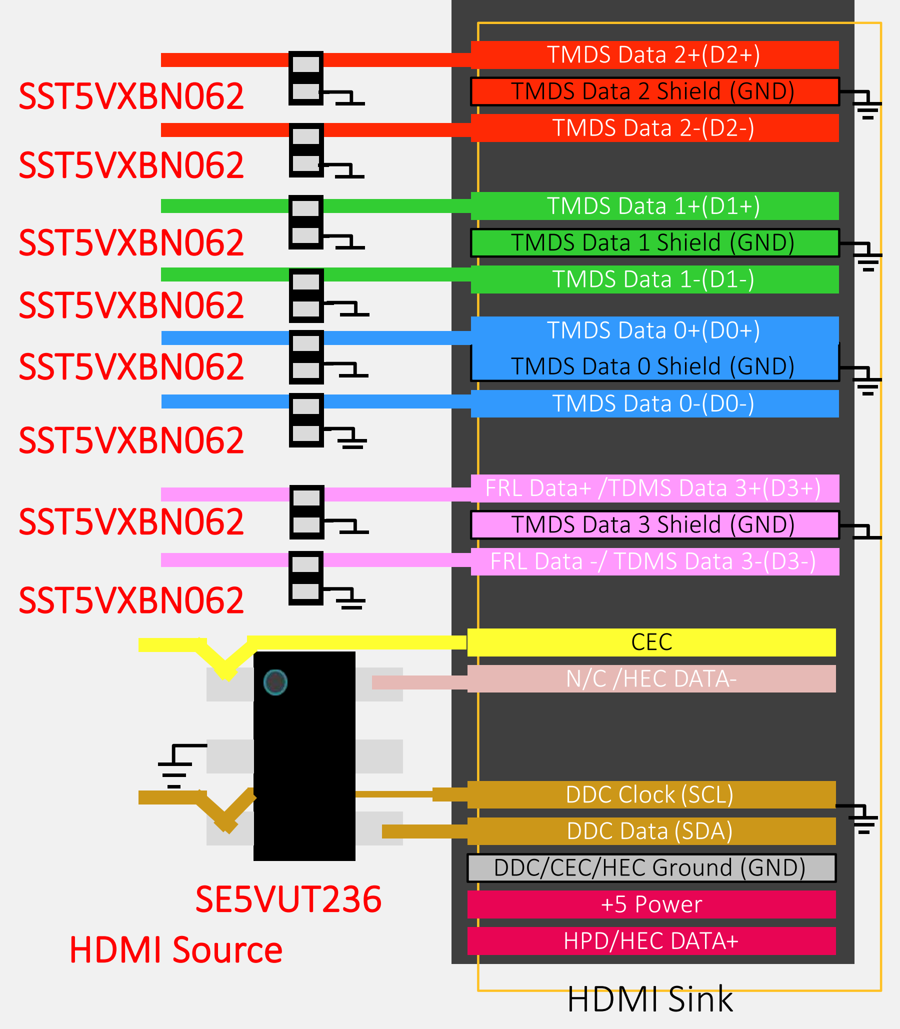
HDMI 2.0 / 2.1 TMDS Application

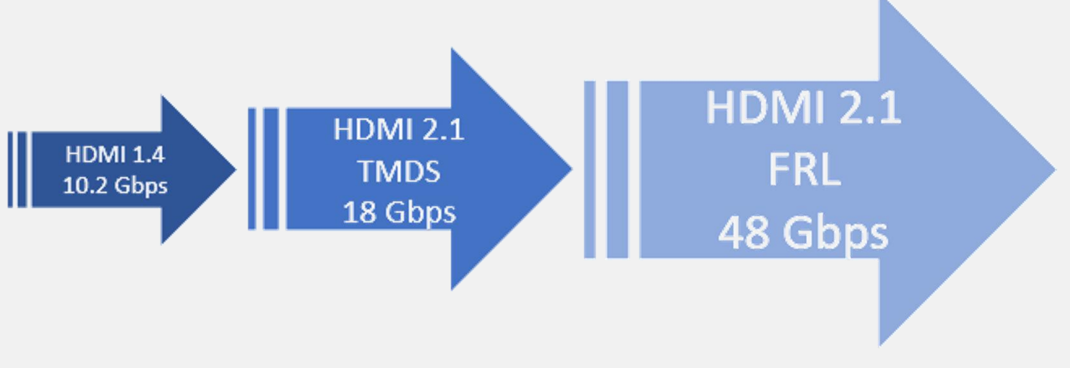


Recommend Part

P/N	Package	lines	Place
SST3V3RN2510	DFN2510-10L	4	TMDS+ , TMDS-
SST5VXBN062	DFN0603-2L	1	TMDS+ , TMDS-
ST5VUHT236	SOT23-6L	4	CEC,SCL,SDA,HEC
SE5VUT236	SOT23-6L	4	CEC,SCL,SDA,HEC

HDMI 2.0 / 2.1 TMDS Application





Recommend Part

P/N	Package	lines	Place
SST5VXBN062	DFN0603-2L	1	TMDS+ , TDMS-,FRL
ST5VUHT236	SOT23-6L	4	CEC,SCL,SDA,HEC
SE5VUT236	SOT23-6L	4	CEC,SCL,SDA,HEC

Focus Products

SSGSEMI P/N	PKG	Vrwm^{MAX} (V)	V_{BR}^{MIN} (V)	C_J^{TYP} (pF)	CH	Direction	ESD^{C} (kV)	ESD$_{A}$ (kV)	Ipp$^{8/20, 2\Omega}$ (A)	MPQ	
SST1V2XBP062	CSP0603-2L	1.2	-	0.25	1	Bi	±15	±20	4	10K	NEW
SST3V3XBN062	DFN0603-2L	3.3	4.5	0.2	1	Bi	±30	±30	9	10K	NEW
SST5VXBN062	DFN0603-2L	5	5.5	0.2	1	Bi	±30	±30	9	10K	NEW
SSE1V8UBN102	DFN1006-2L	1.8	3.3	0.5	1	Bi	±30	±30	7	10K	NEW
ST4V5FBHN102	DFN1006-2L	4.5	4.7	70	1	Bi	±30	±30	45	10K	
ST5VFBHN102	DFN1006-2L	5	5.5	200	1	Bi	±30	±30	100	10K	
ST7VFHN102	DFN1006-2L	7	7.2	280	1	Uni	±30	±30	45	10K	
ST12VFHN102	DFN1006-2L	12	14	50	1	Uni	±30	±30	50	10K	
ST20VFN102	DFN1006-2L	20	22	100	1	Uni	±30	±30	50	10K	NEW
SST2V5UN208	DFN2010-8L	2.5	3.5	0.8	2	Uni	±30	±30	19	10K	NEW
SEO12VLN205	DFN2020-5L	12	13.3	18	2	Uni	±30	±30	100	10K	NEW
SSE3V3LT236	SOT23-6L	3.3	3.6	3.8	4	Uni	±30	±30	25	3K	NEW
SE5VUT236	SOT23-6L	5	6.8	0.45	4	Uni	±26	±27	3.5	3K	
ST5VRN2510	DFN2510-10L	5.5	6.8	0.4	4	Uni	±25	±25	3.5	3K	
SST3V3RN2510	DFN2510-10L	3.3	3.6	0.3	4	Uni	±20	±30	3	3K	
SST2V5LN3010	DFN3020-10L	2.5	3.0	3	4	Uni	±30	±30	40	3K	NEW

SST1V2XBP062

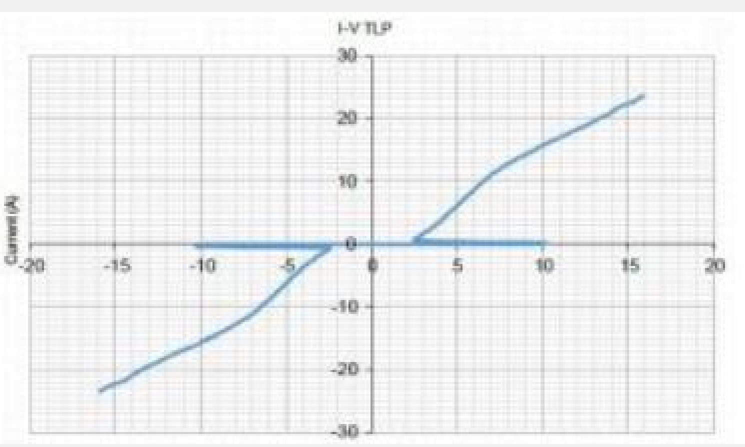
Features

- Ultra-low capacitance : 0.25pF (typ.)
- Reverse working voltage : 1.2V
- IEC 61000-4-2 (Air) : ±20kV
- IEC 61000-4-2 (Contact) : ±15kV
- IEC 61000-4-5 (Surge) : 4A (8/20us)

Application

- USB 3.2 Gen 1 and Gen 2
- RF antenna
- Display port
- Ethernet 10G BASE-T
- LVDS

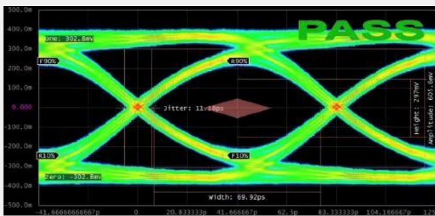
TLP Curve



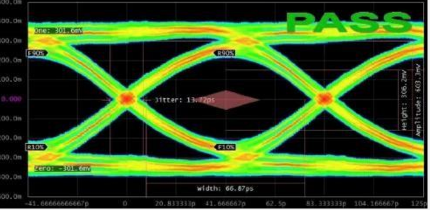
Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ.	Max	Unit
V_{RWM}	Reverse working voltage					1.2	V
V_{TRIG}	Trigger voltage				9.5		V
V_H	Lower voltage than V_H guarantees the protection turn-off			1.2	1.7		V
I_{HOLD}	Minimum on-state current				35		mA
I_{RM}	Leakage current	V_{RWM} =1.2V				10	nA
V_{CL}	Clamping voltage	I_{pp} = 4 A, 8/20 us			4	5	V
		8 kV contact discharge after 30 ns, IEC 61000-4-2			11		
		TLP measurement (pulse duration 100 ns)	I_{PP} = 16 A		10		
			I_{PP} = 4 A		4		
R_{DYN}	Dynamic resistance	TLP pulse duration 100 ns (from 4A to 16 A I_{pp})			0.5		Ω
C_{LINE}	Line capacitance	V_{LINE} = 0 V, F = 3 GHz			0.28	0.35	pF
		V_{LINE} = 0 V, F = 10 GHz			0.25	0.33	
f_C	Cut-off frequency	-3dB			24		GHz

Test pattern @12Gbps



w/o SST5VXBN062



w/ SST5VXBN062

CSP0603-2L

SST5VXBN062

Features

- Ultra-low capacitance : 0.2pF (typ.)
- Reverse working voltage : 5.0V
- IEC 61000-4-2 (Air) : ±30kV
- IEC 61000-4-2 (Contact) : ±30kV
- IEC 61000-4-5 (Surge) : 9A (8/20us)

Application

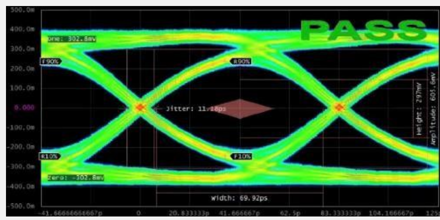
- USB3.2/USB4.0
- HDMI 2.0/2.1

TLP Curve

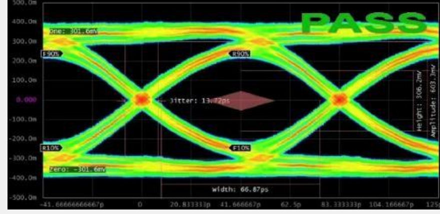
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{RWM}	Reverse Working Voltage				5	V
I_R	Reverse Leakage Current	$V_R = 5V$		100	200	μA
V_{BR}	Breakdown Voltage	$I_{t1} = 1mA$	5.5	10		V
V_H	Holding Voltage	$I_H = 100mA$	1.2			V
V_C[1]	Clamping Voltage	$I_{PP} = 9A$, $t_P = 8/20\mu s$		6		V
		$I_{TLP} = 16A$, $t_P = 10/100ns$		6		V
R_{DYN}[1, 2]	Dynamic Resistance	$t_P = 10/100ns$		0.23		Ω
C_J[1]	Junction capacitance	$V_R=0V, f=1MHz$		0.20	0.25	pF
		$V_R=0V, f=1GHz$		0.18	0.20	pF

Test pattern @12Gbps



w/o SST5VXBN062



w/ SST5VXBN062

DFN0603-2L

SSE1V8UBN102

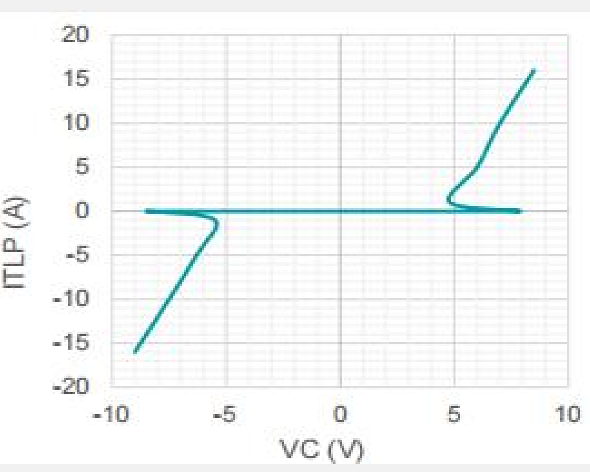
Features

- Low capacitance: 0.5pF(typ.)
- Reverse standoff voltage: 5V
- IEC 61000-4-2 (Air): ±30kV
- IEC 61000-4-2 (Contact): ±30kV
- IEC 61000-4-5 (Surge): 7A (8/20us)

Application

- Serial ATA
- PCI Express
- Display port

TLP Curve

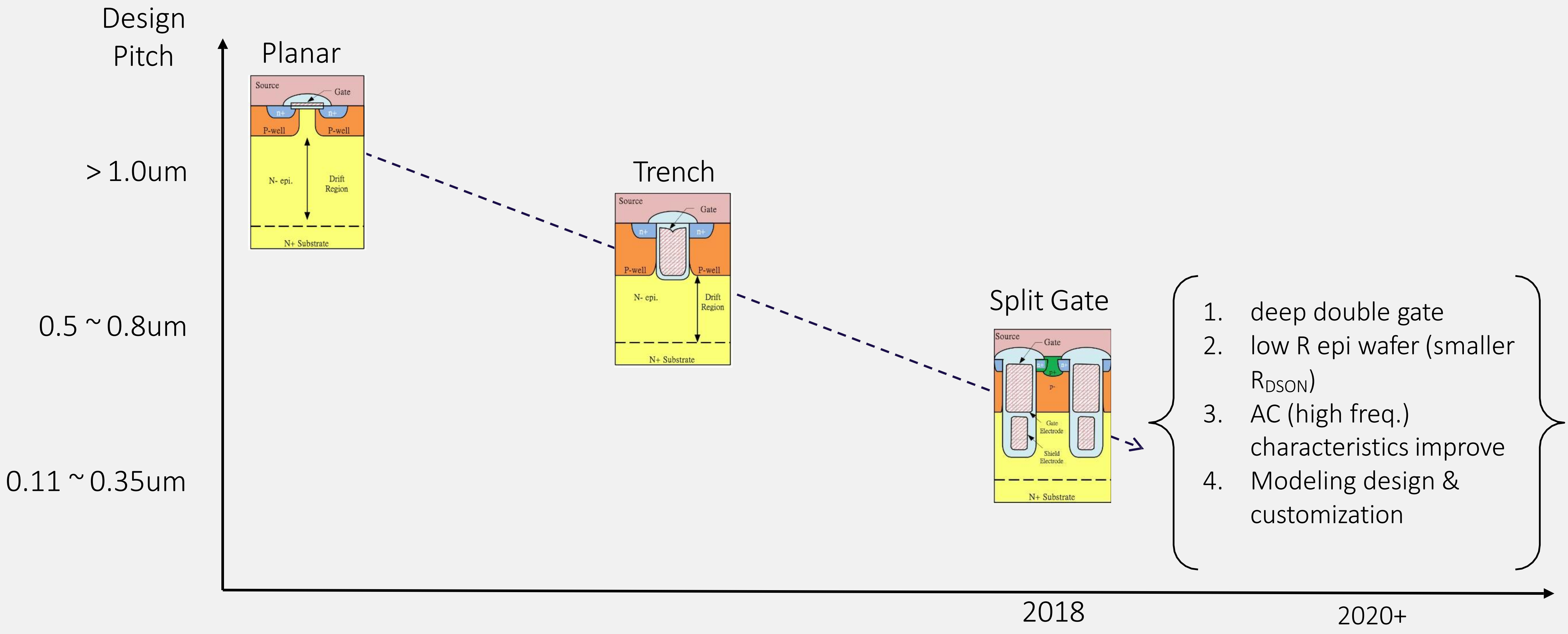


Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse working voltage	V_{RWM}				1.8	V
Holding voltage	V_H	I_H = 100mA		3.6		V
Reverse leakage current	I_R	V_{RWM} = 1.8V			10	nA
Clamping voltage (8/20us)	V_C	I_{PP} = 7A		8.0		V
Clamping voltage (10/100ns)	V_C	I_{TLP} = 16A		8.0		V
Dynamic resister	R_{DYN}	tp = 10/100ns		0.25		Ω
Junction capacitance	C_J	V_R = 0V, f = 1 MHz		0.5	0.7	pF

DFN1006 - 2L

MOSFET Technology Roadmap



SSE3V3LT236

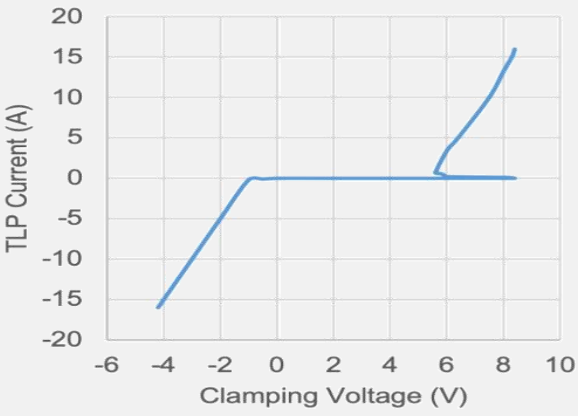
Features

- Ultra-low capacitance : 3.8pF (typ.)
- Reverse working voltage : 3.3V
- IEC 61000-4-2 (Air) : ±30kV
- IEC 61000-4-2 (Contact) : ±30kV
- IEC 61000-4-5 (Surge) : 25A (8/20us)

Application

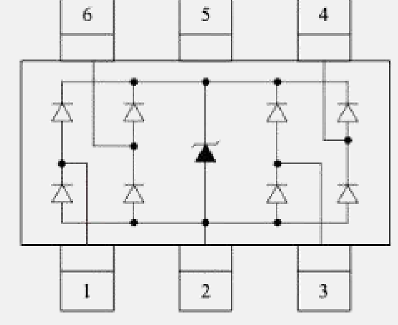
- Ethernet
- Switching Systems
- Telecom equipment

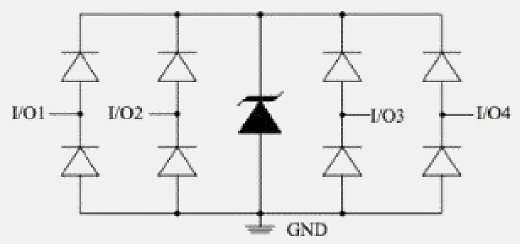
TLP Curve



Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{RWM}	Reverse working voltage	I/O Pin to GND			3.3	V
I_R	Reverse leakage current	V_{RWM} = 3.3V; Any I/O to GND			100	nA
V_h	Holding Voltage	I_h=10mA	3.5			V
V_C	Surge Clamping Voltage (tp=8/20us) Any I/O Pin to GND	I_{PP} = 1A			5.5	V
		I_{PP} = 10A			10.5	V
		I_{PP} = 20A			18.0	V
C_J	Junction Capacitance	V_R = 0V, f = 1 MHz, I/O to GND		3.8	5.0	pF
		V_R = 0V, f = 1MHz, between I/O Pins		2.0	2.5	pF





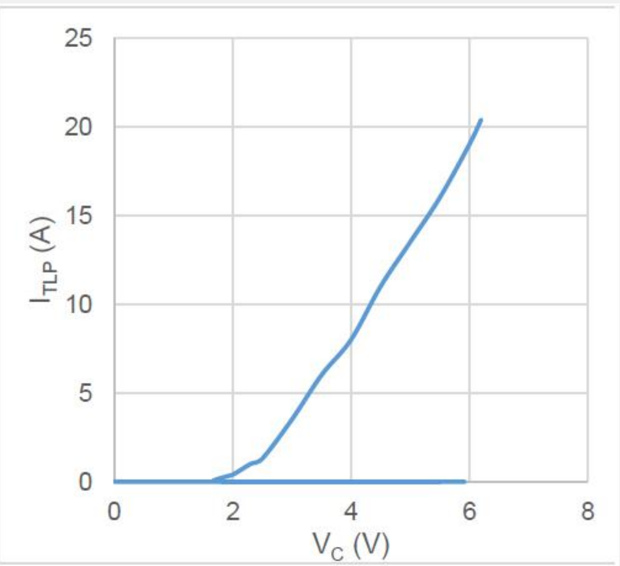
SOT-23-6L

SST2V5UN208

Features

- Low capacitance: 0.8pF(typ.)
- Reverse working voltage: 2.5V
- IEC 61000-4-2 (Air): ±30kV
- IEC 61000-4-2 (Contact): ±30kV
- IEC 61000-4-5 (Surge): 19A(8/20us)

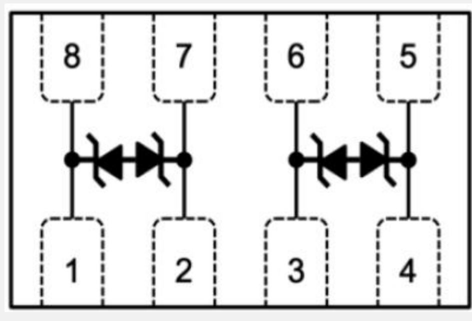
TLP Curve



Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{RWM}	Reverse Working Voltage	Any I/O to I/O	-2.5		2.5	V
V_{BR}	Breakdown Voltage	I_R = 2uA; Differential Line Pair	3.5	5.0		V
I_R	Reverse Leakage Current	V_{RWM}=2.5V;Each Line			1	μA
V_C	Surge Clamping Voltage (8/20us)(Positive)	I_{PP} = 5A, Differential Line Pair		3.0		V
		I_{PP} = -5A, Differential Line Pair		3.0		V
V_C	TLP Clamping Voltage (tp =100ns,tr = 1ns) (Positive)	I_{TLP}= 16A, Differential Line Pair		5.45		V
		I_{TLP}= -16A, Differential Line Pair		5.45		V
R_{DYN}	TLP Dynamic Resistance (tp=100ns, tr=1ns)	Differential Line Pair (Positive)		0.2		Ω
C_J	Junction Capacitance	V_R = 0V, f = 1 MHz, Differential Line Pair			0.8	pF
		V_R = 2.5V, f = 1 MHz, Differential Line Pair			0.7	

Graphic symbol



DFN2010-8L

Package

SST3V3RN2510

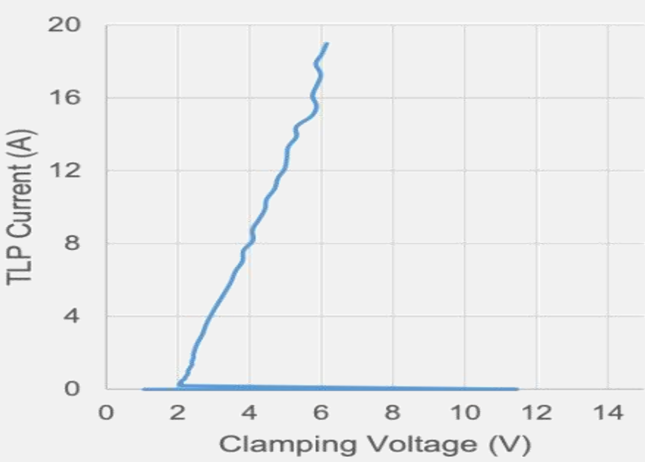
Features

- Ultra-low capacitance : 0.28pF (typ.)
- Reverse working voltage : 1.8V
- IEC 61000-4-2 (Air) : ±15kV
- IEC 61000-4-2 (Contact) : ±12kV
- IEC 61000-4-5 (Surge) : 6A (8/20us)

Application

- V-by-One
- Type-C/USB3.2/USB4.0
- HDMI 2.1
- e-SATA

TLP Curve



Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{RWM}	Reverse working voltage				3.3	V
V_{TRIG}	Triggering voltage			8.5	10	V
V_h	Holding voltage	I_h = 40mA		1.8		V
I_R	Reverse leakage current	V_{RWM} = 3.3V		5	100	nA
V_C	Surge Clamping voltage	I_{PP} = 3A		3.8		V
V_C	TLP Clamping voltage	I_{PP} =16A		8.0		V
R_{DYN}	Dynamic resistance			0.40		Ω
C_J	Junction capacitance	V_R = 0V, f = 1 MHz		0.40		pF
		f = 3Ghz		0.30		
f_C	Cut-off frequency at -3dB			10		GHz

Test pattern @10Gbps

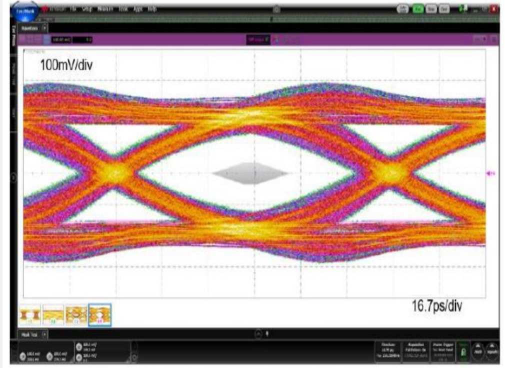
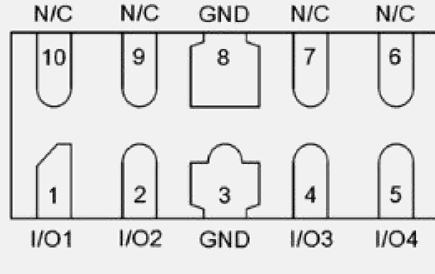
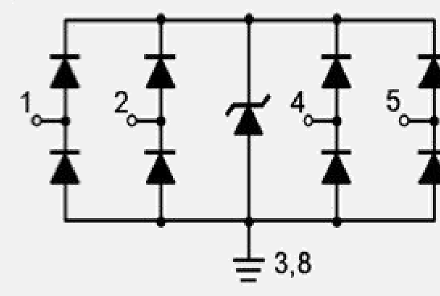


Fig6. USB3.1 Gen 2, 10.0 Gbps eye diagram without SST3V3RN2510

Fig7. USB3.1 Gen 2, 10.0 Gbps eye diagram with SST3V3RN2510



DFN2510-10L



SEO12VLN205

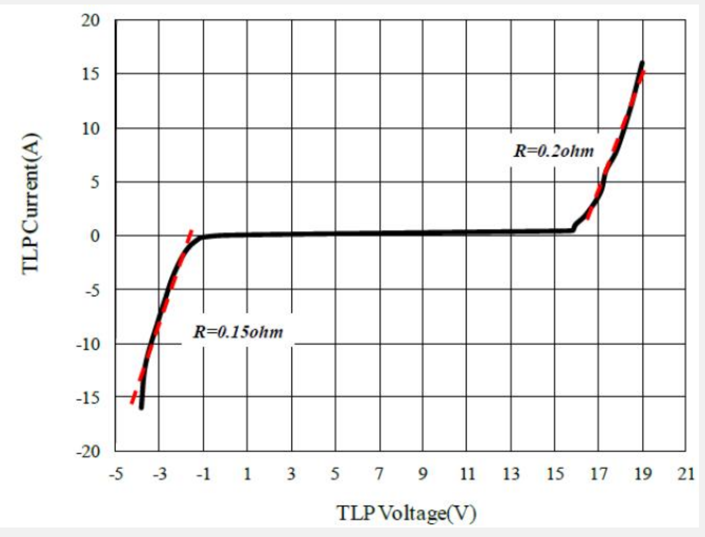
Features

- Low capacitance: 6pF(typ.)
- Reverse working voltage: 12V
- IEC 61000-4-2 (Air): ±30kV
- IEC 61000-4-2 (Contact): ±30kV
- IEC 61000-4-5 (Surge): 100A(8/20us)

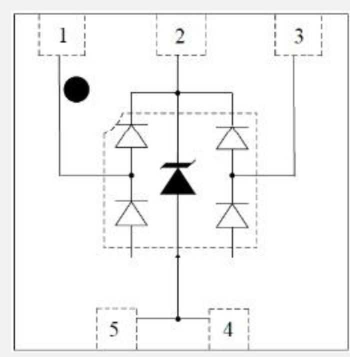
Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{RWM}	Reverse working voltage		-	-	12	V
V_{BR}	Breakdown voltage	I_t= 1mA Pin1,2 or 3 to Pin 4,5 and (2)	13.3	-	18	V
I_R	Reverse leakage current	V_{RWM} = 12V Pin1,2 or 3 to Pin 4,5 and (2)	-	0.01	0.1	μA
V_C (1)	Surge Clamping Voltage	I_{PP} = 100A, t_p=8/20us Pin1,2 or 3 to Pin 4,5 and (2)	-	30	35	V
		I_{PP} = 16A, t_p=10/100us Pin1 or 3 to Pin 4,5 and (2)	-	19	-	V
R_{DYN} (1)		t_p= 10/100ns (TLP) (3) Pin1 or 3 to Pin 4,5 and (2)	-	0.2	-	Ω
C_{ESD} (1)	Parasitic Capacitance	VR= 0V, f = 1MHz Pin1 or 3 to Pin 4,5 and (2)	-	6	12	pF

TLP Curve



Graphic symbol



Package

DFN2020-5L

SST2V5LN3010

Features

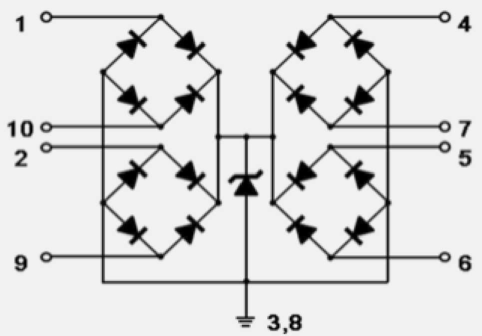
- Low capacitance: 3pF(typ.)
- Reverse working voltage: 2.5V
- IEC 61000-4-2 (Air): ±30kV
- IEC 61000-4-2 (Contact): ±30kV
- IEC 61000-4-4 (EFT): 40A(5/50ns)
- IEC 61000-4-5 (Surge): 40A(8/20us)

TLP Curve

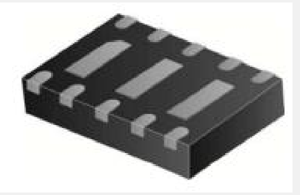
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{RWM}	Reverse Working Voltage	Any I/O to GND			2.5	V
V_{t1}	Trigger Voltage	$I_{t1} = 1\mu A$	3.0	3.7	4.5	V
V_H	Holding Voltage	I_R = 1 mA; I/O to GND	3.0		4.0	V
I_R	Reverse Leakage Current	V_{RWM}= 2.5V; I/O to GND		0.1	1	μA
V_C	Surge Clamping Voltage (8/20us) (Positive)	I_{PP} = 1A, Any I/O to GND [1]			4.5	V
		I_{PP} = 10A, Any I/O to GND [1]			7.5	V
		I_{PP} = 25A, Any I/O to GND [1]			12	V
		I_{PP} = 40A, Two I/O to GND [2]			20	V
V_C	TLP Clamping Voltage(10/100ns) (Positive)	I_{TLP} = 1A, Any I/O to GND [1]		5.8		V
		I_{TLP} = 15A, Any I/O to GND [1]		7.5		V
		I_{TLP} = 1A, I/O to I/O [3]		5.5		V
		I_{TLP} = 16A, I/O to I/O[3]		11		V
R_{DYN}	TLP dynamic resistance (tp=100ns, tr=1ns)	I/O to GND (Positive)		0.19		Ω
		I/O to GND (Negative)		0.2		Ω
		I/O to I/O (Positive)		0.19		Ω
C_J	Junction Capacitance	V_R = 0V, f = 1 MHz, I/O to GND		3.0		pF
		V_R = 0V, f = 1 MHz, Between I/O pairs[3]		1.0	1.8	pF

Graphic symbol



Package



DFN3020-10L

Keyboard mouse

#USB2.0 #Vbus Protection #small package #GPIO

SSGSEMI Solution in USB 2.0

Official name		Origin Name	Logo	Data rate(bit)	Theoretical speed (Byte)	Prisilicon P/N
USB 2.0	LowSpeed	USB 1.0	CERTIFIED USB	1.5Mbps	0.1875MB/s	SE5VFBD522 SE5VLBN102
	FullSpeed	USB 1.1		12Mbps	1.5MB/s	
	HiSpeed	USB 2.0	HI-SPEED CERTIFIED USB	480Mbps	60MB/s	SE5VLBN062 SE5VUBN062

Brief Electronic Spec.

P/N	Package	Vrwm(V)	Cj(pF)	Vc(V)@1A	Ipp(A) Max	ESD contact	ESD Air	place
SE5VFBD522 SE5VFBN102 SE5VFBN062	SOD523 DFN1006-2L DFN0603-2L	5V	12pF	9V	8A	±30kV	±30kV	D+ , D- Vbus
SSE5VLBN102 SSE5VLBN062	DFN1006-2L DFN0603-2L	5V	1pF	6.2V	11A	±30kV	±30kV	D+ , D- Vbus
SE5VUBN062	DFN0603-2L	5V	0.5pF	11V	4A	±15kV	±15kV	D+ , D-

SSGSEMI Solution in GPIO

Brief Electronic Spec.

P/N	Package	Vrwm(V)	Cj(pF)	Vc(V)@1A	Ipp(A) Max	ESD contact	ESD Air	place
SE3V3FBD522 SE3V3FBN102 SE3V3FBN062	SOD523 DFN1006-2L DFN0603-2L	3.3V	10pF	5V	8A	±30kV	±30kV	
SE3V3UBN102 SE3V3UBN062	DFN1006-2L DFN0603-2L	3.3V	0.35pF	12V	4A	±25kV	±25kV	
SE3V3FBN062	0201-2L	3.3V	20pF	5.5V	10A	±30kV	±30kV	

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Thank You